IN THE DRAWINGS

The Examiner has indicated that the drawings filed on July 21, 2004 have been accepted.

REMARKS

Claims 2-3 have been amended. Claims 1-44 are currently pending in the patent application.

The Examiner allowed claims 28-44, and indicated claims 11, 13 and 15-27 would be allowable if rewritten in independent form.

The Examiner objects to the title of the invention as not being descriptive, and suggests that the phrase "using a digital filter and hysteresis adjuster" be added to the title. The Applicants respectfully disagree with the Examiner's suggestion, as the title proposed by the Examiner covers only some of the disclosed embodiments, and is thus viewed as unnecessarily restrictive. For example, the Examiner has properly noted that claim 13 is allowable. Claim 13 is directed to a use of a hysteresis, but not necessarily a digital filter. Similarly, other disclosed embodiments include other features that may or may not include a hysteresis and/or a digital filter. The Applicants thus submit that the original title "A Phase Detector for Reducing Noise" is more representative of the various disclosed embodiments.

The Examiner rejects claims 1-10 and 12 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 6,489,823 (*Iwamoto*). The Applicants respectfully traverse this rejection. Claim 1, among other things, calls for a second circuit adapted to receive a first signal, to receive a second signal, and to modify the second signal based upon the control signal. Claim 1 further specifies that the second circuit is adapted to provide the first signal and the modified second signal as input signals to the phase detector. Thus, this claim feature specifies that at least two

signals (*i.e.*, a first signal and a second signal) are provided by the second circuit as input signals to the phase detector.

The Examiner argues that claim 1 is taught by Figure 18 of Iwamoto. In particular, the Examiner argues that the "second circuit" of claim 1 corresponds to elements 222, 223, and 226 of Figure 18 of Iwamoto, and that this second circuit provides the first signal and the modified second signal as input signals to the phase detector 228. *See* Office Action, page 3. The Examiner argues that the first signal is a form of a delayed ECLK signal and the modified second signal is the output of element 223. A brief review of Figure 18 of Iwamoto, the figure on which the Examiner relies for his rejection, reveals the shortcoming in the Examiner's argument. Figure 18 shows that only one signal, namely the ICLK (the output of element 223), is provided to the phase detector 228. However, in applying Iwamoto, the Examiner simply ignores that claim 1 calls for providing input signals (the first signal and the modified second signal) to the phase detector. In Iwamoto, the elements 222, 223, and 226 (which the Examiner asserts correspond to the "second circuit") only provide RCLK to the phase comparator 228. Thus, contrary to the Examiner assertion, Iwamoto at least does not teach providing the first signal and the modified second signal as input signals to the phase detector. Accordingly, for this reason alone, claim 1 and its dependent claims are allowable.

The Examiner rejects Claim 14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 5,642,082 (*Jefferson*). The Applicants respectfully traverse this rejection. Claim 14 calls for receiving a clock signal and receiving a feedback signal formed using the clock signal. Claim 14 further calls for generating a control signal indicative of a phase difference between the

clock signal and the feedback signal and modifying the feedback signal based upon the control signal.

The Examiner argues that Figure 7 of Jefferson teaches the features of claim 14. Specifically, with respect to the claimed feature of generating a control signal indicative of a phase difference between the clock signal, the Examiner argues that Jefferson teaches a control signal (reset 147) indicative of a phase difference (UP and DWN) between the clock signal (REFCLK) and the feedback signal (output of 20). *See* Office Action, page 4. The Applicants respectfully disagree with the Examiner's contention that Jefferson anticipates claim 14. As recited, claim 14 calls for generating a control signal indicative of a phase difference. In Jefferson, however, the reset signal 147 (which the Examiner asserts corresponds to "control signal") is not based on the phase difference (*e.g.*, the UP/DWN signals). A closer study of Jefferson, and specifically of Figure 2 and the accompanying description, reveals the flaw in the Examiner's argument.

Figure 2 of Jefferson provides a detailed view of the element 100 of Figure 7, and is helpful in illustrating that the UP/DWN signals of PFD 12 have no relation to the reset signal 147. Figure 2 shows that the reset signal 147, which is based on outputs of the flip-flops (and not the UP/DWN signals), is used to indicate that voltage UF has either risen to VCC-A, or has fallen to VSS+B. *See* Jefferson, col. 5, lines 3-7. As explained in Jefferson, and as confirmed by the circuitry illustrated in Figure 2, the UP/DWN signals of PFD 12 are respectively used to charge pump 14 to decrease the charge in low-pass filter and to charge pump 14 to increase the charge in the low-pass filter 16. *Id.* at col. 4, lines 6-34. Thus, contrary to the Examiner's

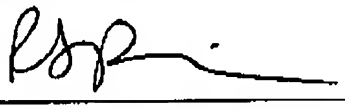
assertion, the reset signal 147 is not indicative of a phase difference (UP/DWN) between the clock signal and the feedback signal. Indeed, a close analysis of Jefferson confirms this point. As such, Jefferson at least does not teach the claimed "generating" feature. For this reason alone, claim 14 is allowable.

Claim 14 is allowable for an additional reason. The Examiner asserts that Jefferson teaches the claimed feature of modifying the feedback signal based upon the control signal because it discloses the UP/DWN signal being modified by the reset signal 147 (which corresponds to the control signal, according to the Examiner). The Applicants respectfully disagree. The Examiner's rejection is erroneous. The Examiner initially contends that the "feedback signal" of claim 14 corresponds to the output signal of element 20, which is a fixed delay circuit in Figure 7. *See* Office Action, page 4. However, when it comes to applying Jefferson to the later-recited "modifying" claimed feature, the Examiner takes an inconsistent position and argues the "feedback signal" is a form of UP/DOWN signal (as opposed the output signal of element 20 he alleged earlier). In Jefferson, the output signal of element 20 (which the Examiner initially asserts corresponds to the "feedback signal" of claim 14) is not modified based on the reset signal (*i.e.*, the "control signal," according to the Examiner). Rather, Jefferson explains, at col. 6, lines 31-32 that the reset signal 147 causes the output signals (UP/DWN) of the PFD 12 to be disabled. Thus, the reset signal 147 disables PFD 12, and does not modify the feedback signal (i.e., the output of element 20), as alleged by the Examiner. Accordingly, Jefferson does not teach the claimed feature of modifying the feedback signal based upon the control signal. For this additional reason, claim 14 is allowable.

Arguments with respect to other dependent claims have been noted. However, in view of the aforementioned arguments, these arguments are moot and therefore not specifically addressed. To the extent that characterizations of the prior art references or Applicants' claimed subject matter are not specifically addressed, it is to be understood that Applicants do not acquiesce to such characterization.

In light of the arguments presented above, Applicants respectfully assert that the pending claims are allowable. Accordingly, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas, telephone number (713) 934-4060 to discuss the steps necessary for placing the application in condition for allowance.

Date: March 14, 2005	Respectfully submitted, WILLIAMS, MORGAN & AMERSON, P.C. CUSTOMER NO. 23720 By:  Ruben S. Bains, Reg. No. 46,532 10333 Richmond, Suite 1100 Houston, Texas 77042 (713) 934-4064 (713) 934-7011 (facsimile) ATTORNEY FOR APPLICANT(S)